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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,927	08/03/2007	**Irwin Aberin**	1431.168.101/FIN 581 PCT/	9898

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EXAMINER	
JUNG, MICHAEL	

ART UNIT	PAPER NUMBER
2895	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,927	ABERIN ET AL.	
	Examiner	Art Unit	
	MICHAEL JUNG	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 21-23 are objected to because of the following informalities:

Regarding claim 21, add --forming-- between "before" and "a plurality of upper contact traces" in lines 1-2.

Regarding claim 22, "the redistribution board" lacks antecedent basis. Change "the redistribution board" to --the substrate--.

Regarding claim 23, change "substrate" to --the substrate" and "mold" to --a mold--.

Regarding claim 24, "the substrate" lacks antecedent basis. Change "the substrate" to --the sheet--.

Regarding claim 30, delete a comma after "a plurality of chip contact areas".

Regarding claim 32, "the flip-chip technique" lacks antecedent basis. Change "the flip-chip technique" to --a flip-chip technique--.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 17-21, 24-29 and 33-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Each of the claims 17, 24 and 33 recites a limitation "will be". Such limitation is indefinite because it imports a contingency that may or may not occur. For the purposes of the examination, the limitation "will be" will be, no pun intended, interpreted as meaning --is-- or --are-- depending on whether the subject is singular or plural.

Claim Rejections - 35 USC § 102

3. Claims 17-19, 24-28 and 30-32 rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,014,318 A to Takeda.

Regarding claim 17, Takeda teaches a method comprising:

providing a substrate 1 comprising a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material") and a plurality of upper contact traces 22 (col. 4, ln 66 - col. 5, ln 4 - "The wiring substrate 1 is a multi-layer substrate...and is constituted of a conductive wiring..."; Fig. 6 designates the signal wiring 11 and the conductive wiring 22 with the same shade (blank).), upper contact pads 12 (col. 6, ln 24 - 36 - "At Fig. 11, the wiring substrate 1 is like the same as the first example of the embodiment of the present invention....however for the connection between the semiconductor chip 2 and the wiring substrate, a metal wire is not used, a bump 12...is formed and the wiring substrate 1 is connected to electrodes of the semiconductor chip...") on the upper surface of the substrate 1, a second plurality of lower conducting traces 11 (col. 4, ln 55-65 - "signal wiring 11) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on the bottom surface of the substrate 1 (see Fig. 11) and conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces 22 and lower conducting traces 11 (compare Figs. 6 and 11);

forming a plurality of non-plated vent holes 7 (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist..."; Fig. 11 shows an absence of a plating on the perimeter of the vent holes.) in the substrate 1 in an area in which a semiconductor chip 2 is mounted to the upper surface (Fig. 11 shows a plurality of vent holes directly underneath the semiconductor chip 2.) and in areas of the substrate which are adjacent to the area in which the semiconductor chip is mounted (Fig. 11 shows a plurality of vent holes that are disposed in a perimeter area of the semiconductor chip 2; col. 5, ln 8-19); and

covering the upper and lower surfaces of the substrate 1 by a layer of solder resist 5 (see Fig. 11) leaving the contact areas 10 free from solder resist 5 (Fig. 11 shows the ball electrode terminals that are not covered by the solder resist 5).

Regarding claim 18, Takeda further teaches the vent holes 7 that are closed at one end by a layer of solder resist 5 on the upper surface of the substrate 1 (see Fig. 11).

Regarding claim 19, Takeda further teaches the vent holes 7 that include solder resist (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist...").

Regarding claim 24, Takeda teaches a substrate 1 comprising:

a sheet 1 of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material");

a plurality of upper conducting traces 22 (col. 4, ln 66 - col. 5, ln 4) and upper contact pads 12 (col. 6, ln 24 - 36) on an upper surface of the sheet 1, a second plurality

of lower conductive traces 11 (col. 4, ln 55-65 - "signal wiring 11) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on a bottom surface of the sheet 1 and a plurality of conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces 22 and lower conducting traces 11 (compare Figs. 6 and 11);

a plurality of non-plated vent holes 7 in the substrate in an area in which a semiconductor chip 2 is mounted to the upper surface (Fig. 11 shows a plurality of vent holes directly underneath the semiconductor chip 2.) and in areas of the substrate which is adjacent to the area in which the semiconductor chip 2 is mounted (Fig. 11 shows a plurality of vent holes that are disposed in a perimeter area of the semiconductor chip 2; col. 5, ln 8-19); and

a layer of solder resist 5 covering the upper and lower surfaces of the substrate leaving the contact areas 10 free from solder resist 5 (see Fig. 5).

Regarding claim 25, Takeda further teaches the vent holes 7 that include solder resist (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist...").

Regarding claim 26, Takeda further teaches the vent holes 7 that are closed at one end by a layer of solder resist 5 on the upper surface of the substrate 1 (see Fig. 11).

Regarding claim 27, Takeda further teaches the plurality of vent holes 7 that are laterally located towards the center of the substrate 1 (see Fig. 11).

Regarding claim 28, Takeda further teaches the plurality of vent holes 7 that are laterally located towards the center and towards the outer edges of the substrate 1 (see Fig. 11).

Regarding claim 30, Takeda teaches a semiconductor package comprising:

a sheet 1 of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material");

a plurality of upper conducting traces 22 (col. 4, ln 66 - col. 5, ln 4) and upper contact pads 12 (col. 6, ln 24 - 36) on an upper surface of the sheet 1, a second plurality of lower conductive traces 11 (col. 4, ln 55-65 - "signal wiring 11) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on a bottom surface of the sheet 1 and a plurality of conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces 22 and lower conducting traces 11 (compare Figs. 6 and 11);

a plurality of non-plated vent holes 7 through the sheet 1 (see Fig. 11);

a layer of solder resist 5 covering the upper and lower surfaces of the substrate leaving the contact areas 10 free from solder resist 5 (see Fig. 5); and

a semiconductor chip 2 including an active surface (Fig. 11 shows a surface facing the sheet 1) with a plurality of chip contact areas (col. 6, ln 33-34 - "electrodes of the semiconductor chip"), electrically connected to the sheet 1, wherein non-plated vent holes 7 are distributed below and adjacent to the semiconductor chip (see Fig. 11).

Regarding claim 31, Takeda further teaches the chip 2 that is encapsulated by mold material 3 (col. 6, ln 36-41; see Fig. 11).

Regarding claim 32, Takeda further teaches the chip 2 that is mounted to the sheet 1 by a flip-chip technique (see Fig. 11).

Claim Rejections - 35 USC § 103

4. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda and further in view of US Pub No. 2001/0042908 A1 to Okada et al. (hereinafter "Okada").

Regarding claim 20, Takeda does not disclose the vent holes that are formed by drilling.

However, Okada teaches forming vent holes 16 that are formed by drilling (para [0052]).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide for vent holes of Takeda by drilling as taught by Okada as a matter of design choice in light of Okada's teaching that vent holes can be formed by punching (para [0052]), lasing (para [0064]) and drilling.

Regarding claim 21, Takeda does not disclose forming the vent holes in the core material before forming a plurality of upper contact traces and upper contact pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and depositing conducting vias.

However, Okada teaches forming vent holes 16 in the core material 6 before a plurality of upper contact traces and upper contact pads on its surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and depositing conducting vias (para [0052] - "...the semiconductor device shown in Fig. 5

has a plurality of vent holes (through holes) 16 previously formed in an organic substrate 6...").

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Takeda with forming vent holes in the core material before forming contact traces, contact pads, external contact areas and conducting vias as described above, so as to simply the method of assembling a semiconductor package by not having to form vent holes after forming contact and conducting features described above.

5. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda and further in view of US Pub. No. 2002/0043721 A1 to Weber et al. (hereinafter "Weber").

Regarding claim 22, Takeda teaches a method comprising:

providing a substrate 1 comprising a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material") and a plurality of upper contact traces 22 (col. 4, ln 66 - col. 5, ln 4 - "The wiring substrate 1 is a multi-layer substrate...and is constituted of a conductive wiring..."; Fig. 6 designates the signal wiring 11 and the conductive wiring 22 with the same shade (blank).), upper contact pads 12 (col. 6, ln 24 - 36 - "At Fig. 11, the wiring substrate 1 is like the same as the first example of the embodiment of the present invention....however for the connection between the semiconductor chip 2 and the wiring substrate, a metal wire is not used, a bump 12...is formed and the wiring substrate 1 is connected to electrodes of the semiconductor chip...") on the upper surface of the substrate 1, a second plurality of

lower conducting traces 11 (col. 4, ln 55-65 - "signal wiring 11) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on the bottom surface of the subtrate (see Fig. 11) and conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces 22 and lower conducting traces 11 (compare Figs. 6 and 11);

forming a plurality of non-plated vent holes 7 (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist..."; Fig. 11 shows an absence of a plating on the perimeter of the vent holes.) in the substrate 1 Regarding claim 23, Takeda further teaches the upper surface of the chip 2 and the substrate 1 with a mold material 3 (col. 6, ln 36-41 - "sealing resin 3");

covering the upper and lower surfaces of the substrate 1 by a layer of solder resist 5 (see Fig. 11) leaving the contact areas 10 free from solder resist 5 (Fig. 11 shows the ball electrode terminals that are not covered by the solder resist 5);

providing a semiconductor chip 2 comprising an active surface (Fig. 2 shows an active surface underneath the semiconductor chip 2, the active surface that is connected to bumps 12.) including a plurality of chip contact areas (col. 6, ln 33-36 - " electrodes of the semiconductor chip");

mounting the chip 2 on the upper surface of the substrate by microscopic solder balls 12 (col. 6, ln 32-33 - "a bump 12 using solder") between the chip contacts and upper contact areas 22 (compare Fig. 6 and 11), wherein non-plated vent holes 7 are distributed below and adjacent to the semiconductor chip 2 (see Fig. 11); and

underfilling the area between the chip and the upper surface of the substrate 1 with epoxy resin 3 (col. 6, ln 36-41; see Fig. 11).

Takeda does not specifically disclose performing a solder reflow.

However, Weber teaches performing a solder reflow (para [0008]).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Takeda with performing a solder reflow as taught by Weber, so as to electrically contact the semiconductor chip with circuit traces of the substrate (Weber, para [0008]).

Regarding claim 23, Takeda further teaches covering the upper surface of the chip 2 and substrate 1 with mold material 3 (col. 6, ln 36-41; see Fig. 11).

6. Claims 29 and 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda and further in view of US Patent No. 6,054,755 A to Takamichi.

Regarding claim 29, Takeda does not specifically disclose a diameter of the vent hole.

However, Takamichi teaches vent holes each having a diameter ranging between 0.15 and 0.5 mm (col. 4, ln 23-24).

At the time of the invention, it would have been obvious to modify the vent holes of Takeda with the vent holes having a diameter ranging between 0.15 and 0.5 mm as taught by Takamichi, so as to allow moisture produced during the reflow heating to escape the semiconductor package through the vent holes to prevent delamination (col. 5, ln 14-22).

Regarding claim 33, Takeda teaches a substrate for a semiconductor package comprising:

a sheet 1 of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material") with a bottom surface each covered with a layer of solder resist 5;

a plurality of upper conducting traces 22 (col. 4, ln 66 - col. 5, ln 4) and upper contact pads 12 (col. 6, ln 24 - 36) on the upper surface (see Fig. 11);

a plurality of bottom conductive traces 11 (col. 4, ln 55-65) and external contact areas 10 (col. 4, ln 55-65) on the bottom surface;

a plurality of conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces 22 and bottom conducting traces 11 (see Fig. 11);

a plurality of non-plated vent holes 7 through sheet 1 in a chip mounting area on the sheet 1 where a semiconductor chip 2 is mounted to the upper surface and in areas adjacent to the chip mounting area (see Fig. 11); and a layer of solder resist covering the bottom surfaces except for the contact areas 10 (see Fig. 11).

Takeda does not disclose upper surface of the sheet covered with a layer of solder resist.

However, Takamichi teaches a layer of solder resist 25a (col. 5, ln 11-22) covering an upper surface of a sheet of core material 41 (col. 6, ln 46-51).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the semiconductor package of Takeda with a layer of solder resist covering the upper surface of a sheet of core material as taught by Takamichi, so prevent adhesive agents from flowing into vent holes (Takamichi, col. 5, ln 11-14).

Regarding claim 34, Takeda further teaches the vent holes 7 that include solder resist (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist...").

Regarding claim 35, Takeda further teaches the vent holes 7 that are closed at one end by a layer of solder resist 5 on the upper surface of the substrate 1 (see Fig. 11).

Regarding claim 36, Takeda further teaches the plurality of vent holes 7 that are laterally located towards the center of the substrate 1 (see Fig. 11).

Response to Arguments

Applicant's arguments with respect to claims 17-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

/MICHAEL JUNG/
Examiner, Art Unit 2895

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2895